Machine Learning Based Power Estimation for CMOS VLSI Circuits

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Abstract —Machine learning which is a subset of artificial intelligence, facilitates systems to acquire the learning from data and ameliorate task performance without direct programming. In VLSI (Very Large Scale Integration) design, power estimation predicts how much power integrated circuits will use to enhance performance as well as efficiency. CMOS VLSI circuits, utilizing CMOS (Complementary Metal-Oxide-Semiconductor) technology, are known for low power usage as well as high performance in digital and analog designs. It focuses on building accurate as well as efficient machine learning models to estimate power consumption during the design phase of CMOS VLSI circuits. By training models using simulation data as well as design details, machine learning renders faster and more accurate power predictions as compared to traditional methods ameliorating circuit design as well as efficiency. Supervised learning techniques with regression and classification models constructively enhance prediction accuracy using labelled data. Unsupervised methods like clustering algorithms aid in identifying hidden power consumption patterns in large datasets. Furthermore, the reinforcement learning renders dynamic approaches by facilitating with the most-effective power management techniques through continuous communication with the design framework. These techniques of reinforcement learning will collectively strengthen power estimation in CMOS VLSI circuits.

Keywords **— CMOS VLSI circuits, VLSI (Very Large Scale Integration), CMOS (Complementary Metal-Oxide-Semiconductor), based Built-In Self-Test (BIST).**

I. INTRODUCTION

Power estimation is a significant part of CMOS VLSI (Very Large Scale Integration) circuit design and it serves as a key function to optimize electronic system performance, efficiency, and reliability. The exact power estimation during the design stage is crucial to recognize power bottlenecks, enact successful power-saving practices and it also comply with industry energy efficiency standards. The traditional power estimation techniques like SPICE simulations tend to involve lengthy and cumbersome analyses which become unrealistic as circuit complexity is higher. The techniques also carry inaccuracies caused by approximations and assumptions made in modelling [1]. To overcome these limitations, machine learning presents an attractive alternative through the provision of rapid and accurate power estimation based on data-driven techniques. The machine learning algorithms can accurately forecast power consumption and minimize design iterations and overall efficiency by using large amounts of data and learning from the design parameters and operating conditions [2].

The method combines machine learning methods as well as CMOS VLSI design to develop prediction models that read design parameters and simulation results and estimate power consumption effectively. The process will include collecting design metrics, learning machine learning models through supervised, unsupervised and reinforcement learning algorithms and the models are tested against actual performance data [3].

The block diagram given below describes this process with important steps like data collection, model training, prediction, and verification marked in it. The machine learning model is trained with current data to forecast power consumption for new circuit designs so that designers are able to make decisions early in the design cycle. The integration not only improves the efficiency of design but also enables the creation of power-efficient technologies used in applications from consumer products to high-end computing systems.

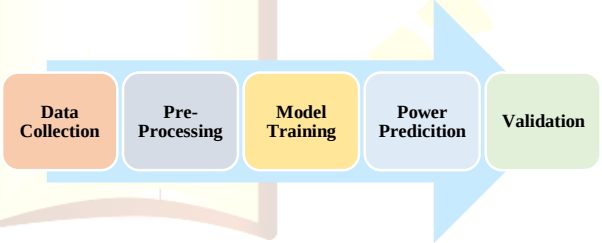

Figure 1 Machine Learning Based Power Estimation for CMOS VLSI Circuits

The figure 1 represents that the machine learning-based power estimation for CMOS VLSI circuits is commenced with data gathering wherein the appropriate design parameters like simulation outputs as well as past power consumption data are obtained.

With a view to create a strong dataset, it is an important step that reflects different circuit designs and conditions. The data collected has normally design specifications, design factors, and performance measurements which are used as inputs to the machine learning model. After data collection, pre-processing is carried out to standardize as well as cleanse the data for consistency and the elimination of any noise or unwanted information. Pre-processing contains processes like data normalization, missing values, and feature extraction which are employed to improve the quality of data which is given as input into the machine learning model and it will also boost power prediction accuracy [4].

After data pre-processing, the model training process initiates by means of machine learning techniques like supervised learning, unsupervised learning and reinforcement learning for building predictive models. The model acquires knowledge from the past data to derive patterns as well as correlations among design parameters and power consumption by means of this process. The trained model is then employed for power prediction by the implementation of learned patterns for prediction of power consumption for innovative models. Validation is the last step here in which the forecasted power estimates are matched with measured values to check the accuracy of the model. This step is critical to fine-tune the model by modifying its parameters and enhancing prediction robustness. A validated model not only provides correct power estimation but also facilitates effective design of CMOS VLSI circuits by eliminating the necessity for rigorous physical testing and repeated simulations [5].

II. Implementation of Artificial Intelligence in VLSI Technology

While implementing Artificial Intelligence in the design of a new high-speed microprocessor, the old way of doing things would mean extensive hand simulations to mitigate process variations and maximize performance. Now, however, AI-powered tools examine historical design data and foretell prospective design problems ahead of time. Machine learning algorithms like neural networks scan for patterns impacting chip yield and performance automatically. While it is being produced, AI software tracks sensor information in real-time, rapidly identifying and fixing abnormalities. AI cuts the design-to-production turnaround dramatically. Eventually, this results in quicker delivery of high-performance, power-saving integrated circuits to customers [6].

Similarly, in a contemporary portable ultrasound machine, IC design using machine learning becomes indispensable to realizing efficient high-image-quality operation. A power-efficient drive circuit of transducers drives ultrasound transducers deep into the tissues. The amplifier is minimized with low-noise amplification in order to enhance echo signals leading to a better ultrasonic echo picture quality. A beamforming circuit coheres signals received at multiple transducers for precise focused image generation in hard human tissue and in hard or difficult cases like bones or complex structures in an embryo. A high-precision analog-to-digital converter (ADC) digitizes such signals. New developments have introduced IC designs that will decrease the device size without sacrificing performance. These advances with implementation of artificial intelligence enable portable ultrasound machines in distant medical facilities. Eventually, these developments enable faster and more precise diagnoses, leading to improved patient care [7].

In designing a next-generation processor chip, conventional VLSI design processes needed extensive manual labor from experts to fine-tune circuit layouts and ensure design integrity. With machine learning (ML) incorporation, Intel and IBM, among other firms, utilize AI-based tools to create designs and validate them automatically. When a new idea for improving power efficiency is presented, ML models review past design data and forecast the optimal layout configurations. Automated CAD software, driven by smart algorithms creates design schematics with less need for human intervention. In testing, ML-based Built-In Self-Test (BIST) systems detect likely faults and test patterns to optimize guaranteeing high-performance capabilities. Predictive analytics shortens the design cycle improving productivity. With reduced manual verification of designs, companies save considerable cost and time-to-market. Finally, this process improves the quality and effectiveness of semiconductor devices, matching the increasing complexity of contemporary electronics [8].

A. Importance of power estimation in VLSI (Very Large Scale Integration) circuit design

Power estimation is one of the most important areas in VLSI (Very Large Scale Integration) circuit design that greatly impacts the optimization of performance, reliability, and efficiency of electronic systems. With increasingly complex and smaller-sized modern electronic devices, precise power estimation ensures designers are able to effectively manage power usage, minimizing heat generation and avoiding thermal problems that can impact device longevity. It assists to attain energy efficiency especially in battery-powered and portable devices where power saving is a concern. In addition, accurate power estimation at the design stage assists in meeting industry standards and regulatory needs for energy-efficient products. It also reduces expensive design iterations by detecting potential power-related issues early in the design cycle and thus speeding up time-to-market and improving the overall competitiveness of the product. This study will present methods for analog-power estimation and it will also demonstrate the practical application to two distinct classes of analog circuits by offering valuable

tools which are used for architectural exploration and high-level system design. These power estimators render power estimates and are based solely on a block's specification values and it will not require detailed circuit implementation knowledge. There are two specific estimators i.e., one for high-speed analog-to-digital converters (ADCs) as well as another for analog continuous-time filters. The ADC power estimator will employ a technology-scalable closed formula delivering first-order results with an accuracy factor of approximately 2.2 across the entire class of high-speed NY Quist-rate ADCs. In contrast, the filter power estimator will adopt a more complex approach by utilizing a rudimentary filter synthesis which is combined with operational Tran's conductor amplifier behavioural models in order to achieve accurate results limited to specific filter implementations [9].

Significance of CMOS (Complementary Metal-Oxide-Semiconductor) technology in modern digital and analog designs: CMOS (Complementary Metal-Oxide-Semiconductor) technology is of particular significance in contemporary digital and analog designs because of its excellent blend of low power usage and high performance. CMOS technology takes advantage of complementary and symmetrical pairs of n-type and p-type MOSFETs allowing for effective switching without much power loss. The fact that CMOS technology is suitable for battery-powered and portable devices where efficiency in energy is the most important factor making it even more significant. CMOS, in digital circuits will yield high-speed processing and less static power consumption which assists in ensuring the longer battery life and lower heat generation. CMOS in analog circuits will ensure low input impedance and low output impedance and thus preserving the signal integrity and the performance of the overall circuit. Its compatibility with high-density integration and scalability will lead to the development of intricate VLSI (Very Large Scale Integration) circuits and drive innovation within consumer electronics, computing, communications, and Internet of Things devices. This study introduces a new CMOS charge pump topology that is able to produce a stable output voltage of 1V over a wide temperature range which is a key challenge in the use of self-powered devices. With the incorporation of a closed-loop regulation circuit, the charge pump created in this work posseses outstanding stability as well as robustness against thermal variations rendering trustworthy operation in variable environments. The integration of a MOSFET-based DC-to-DC converter inside the charge pump also enhances performance through optimized voltage boosting and improved output stability. Extensive simulations validate the practicability of the design indicating that it can be employed in real-world applications for practical uses. This exploration significantly supports to the realization of self-powered equipment's through a robust and efficient voltage regulation under fluctuating temperature environments [10].

B. Challenges associated with traditional power estimation methods in CMOS VLSI circuits

The power estimation methods in CMOS VLSI circuits which are traditional often encounter significant challenges which are mainly because of their reliance on comprehensive as well as time-consuming simulation techniques like SPICE (Simulation Program with Integrated Circuit Emphasis). These methods require precise modelling of complex circuit components as well as detailed analysis of power consumption under varying working conditions and it will result in prolonged design cycles as well as it will also increase computational costs. Since circuit designs become more complex and densely packed, the traditional simulations have difficulty with scalability and it often results in hinderances during the design and testing phases. Moreover, these methods may bring in discrepancies due to approximations as well as assumptions made during the modelling process which will lead to discrepancies between estimated and actual power consumption. Such inaccuracies not only affect the efficiency of the design process but also pose challenges in meeting power efficiency as well as thermal management requirements by highlighting the requirement for more advanced, faster and accurate power estimation techniques in modern VLSI circuit design. The significant challenge in electronic circuit design is power consumption and it is also crucial to address this issue early in the design process for exploring optimal design choices. A typical design flow begins with a high-level system description which will require the accurate power models to guide design decisions. The Power modelling techniques will establish the relationships between power consumption and other performance metrics and it will enable the designers to evaluate trade-offs effectively. In addition to it, efficient power characterization techniques are essential to enhance the accuracy of power estimates. This represents the comprehensive overview of power modeling and estimation techniques, spanning from the register transfer level (RTL) to the transistor level, specifically for FPGA (Field-Programmable Gate Arrays) and ASIC (Application-Specific Integrated Circuits) devices. It also proposes a classification framework for these approaches based on defined metrics, offering designers practical guidance in selecting appropriate methods for their specific design scenarios, even in the absence of a standardized reference across existing studies [11].

C. Requirement for more efficient and accurate predictive techniques to enhance circuit design and efficiency:

The traditional power estimation methods face increasing challenges in maintaining efficiency and accuracy because CMOS VLSI (Very Large Scale Integration) circuits continue to grow in complexity,

The Conventional approaches, such as SPICE (Simulation Program with Integrated Circuit Emphasis) simulations and analytical modeling, often require extensive computational resources and significant time with a view to analyze complex circuits thoroughly. These methodologies may introduce inaccuracies due to approximations as well as assumptions made during the modeling process which will lead to discrepancies between predicted and actual power consumption. In the fast-paced semiconductor industry, where time-to-market is a critical factor these limitations can hinder innovation and can delay the process of product development. Therefore, there is a high requirement for more efficient and accurate predictive techniques that can improve the design process while maintaining high precision in power estimation [12].

The promising solution is offered by machine learning which is a subset of artificial intelligence to resolve these challenges by leveraging data-driven approaches for prediction of power consumption more accurately. Unlike traditional methods, machine learning models have the capability to learn from vast datasets of design parameters and simulation results by enabling them to identify the complex patterns and relationships within the data. These models can render fast as well as accurate power estimates without needing comprehensive simulations by significantly lowering design cycles. Moreover, an advanced machine learning techniques such as supervised learning, unsupervised learning, and reinforcement learning can also adapt to new design scenarios as well as they continuously improve prediction accuracy through iterative learning. By integrating machine learning into the power estimation process, the circuit designers can enhance efficiency by optimizing power management strategies and by expediting the development process of next-generation CMOS VLSI circuits which will contribute to more superior, energy-efficient electronic equipment's [13].

1. Supervised Learning Approaches:

In power prediction for VLSI circuits owing to their capability to learn from labeled data and establish accurate predictive models, the supervised learning approaches have achieved significant attention. The techniques such as linear regression, support vector machines (SVM), decision trees, and deep learning models are commonly employed for this purpose. These models can predict power usage in new circuit designs effectively by training on historical power consumption data along with relevant design and operational parameters.

Supervised learning offers the advantage of leveraging large datasets from simulated or real hardware performance metrics by enabling precise estimations even in complex circuits with numerous transistors and varying workloads. During the design and validation phases of VLSI circuit development, the ability to generalize learned patterns to unseen data makes supervised methods highly valuable.

The predictive accuracy of supervised learning models in VLSI power estimation is highly dependent on the quality and diversity of the training data. Effective feature engineering plays a crucial role in identifying critical attributes such as switching activity, capacitance, voltage levels, and operational frequencies that influence power consumption. Advanced models, particularly neural networks, can also automate feature extraction by improving prediction accuracy in more intricate designs. Furthermore the ensemble methods which can combine multiple supervised learning models have shown promise in reducing prediction errors as well as enhancing model robustness. As VLSI circuits continue to scale down and power efficiency becomes important, the supervised learning approaches offer a scalable as well as adaptive solution for power estimation challenges, contributing to more energy-efficient and optimized semiconductor devices [14].

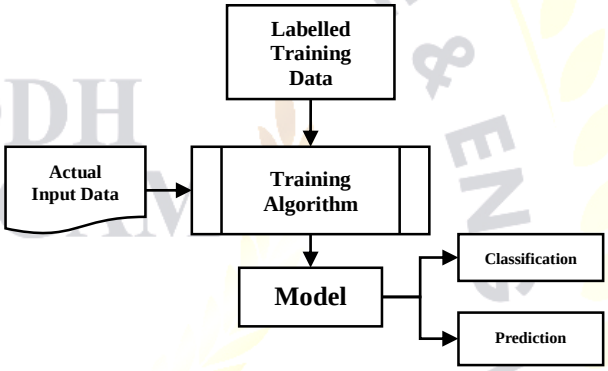

Figure 2: Supervised Learning approach

The figure 2 represents the workflow of a supervised learning approach for predictive modeling. It starts with actual input data which along with labelled training data is fed into a training algorithm. The training algorithm acquire the learning of patterns from the labeled data and creates a model. This trained model is then put in to the actual input data which will lead to two possible outcomes: Classification (where the input data is categorized into predefined classes) as well as Prediction (where the model renders quantitative or probabilistic outputs). This process shows how supervised learning uses historical labeled data to build models that can generalize as well as can create informed predictions on novel data [15].

2. Unsupervised Learning Methods:

An unsupervised learning methods in power estimation of VLSI circuits will focus on identifying hidden patterns as well as structures within power consumption data without relying on labeled datasets. The techniques such as clustering (e.g., K-means, DBSCAN) and dimensionality reduction (e.g., Principal Component Analysis, t-SNE) are often used to analyze power usage patterns and categorize circuit behaviors. An unsupervised models can also assist in identifying the typical power consumption scenarios by grouping similar power profiles which may indicate

inefficiencies or potential design issues. These methodologies are particularly useful during the design exploration phase where they can assist in detecting power anomalies as well as understanding the underlying factors by influencing the power dissipation in complex circuit architectures. In addition to it, by analyzing correlations and redundancies in design parameters, unsupervised learning facilitates feature extraction and selection. Autoencoders, a type of neural network used in unsupervised learning, can compress high-dimensional data into more manageable forms aiding in the analysis of large datasets generated from VLSI design simulations. This process will represent which features have the most significant impact on power consumption and thus streamlining the design process and will also reduce the computational overhead. While unsupervised methods may not provide direct power predictions, they offer valuable insights that can enhance the performance of supervised learning models and support adaptive power management strategies in dynamic operational environments [16].

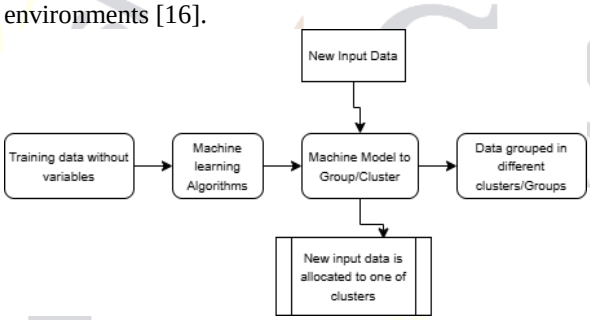

Figure 3: Unsupervised learning

The figure 3 represents the workflow of an unsupervised learning approach, particularly aiming on clustering techniques. It begins with training data without variables specifying the absence of predefined labels or categories. This raw data is then processed using Machine Learning Algorithms which recognize inherent patterns as well as structures within the data. The algorithm generates a machine model to Group/Cluster the data based on similarities as well as differences. When New Input Data is put, the model can allocate this new data to the most suitable cluster. The final output is data Grouped in different Clusters/groups displaying how unsupervised learning effectually organizes data into meaningful clusters without prior labeling, and thus showing hidden patterns as well as insights [17].

3. Reinforcement Learning in VLSI Power Estimation :

In VLSI power estimation, Reinforcement learning (RL) is an emerging approach that includes training an agent with a view to make optimal decisions for minimizing power consumption by interacting with the circuit design environment. As compared to supervised learning, where models learn from labeled datasets, RL includes an agent that learns through trial and error by receiving rewards or penalties based on its actions. The agent could explore different design parameters in the context of VLSI circuits, power management strategies, or hardware configurations to find the optimal settings that will reduce power dissipation. The illustration can be taken as that in dynamic voltage and frequency scaling (DVFS) scenarios, an RL agent can dynamically adjust the voltage as well as frequency of a circuit component to obtain the balance between performance and power efficiency. In power estimation for VLSI circuits, the adaptability of reinforcement learning is particularly beneficial under varying workloads as well as operating conditions. The reinforcement learning model can continuously learn and adapt by offering real-time power management solutions because circuits are subjected to diverse applications and processing demands are also fluctuating. Furthermore, advanced techniques like deep reinforcement learning (DRL) combine the decision-making capabilities of RL with the pattern recognition strengths of deep learning by enabling the agent to handle complex, high-dimensional state spaces typical in modern VLSI systems. Even if RL-based methods often require extensive training as well as computational resources, their potential to automate power optimization and adapt to new scenarios will make them a promising direction for future research in low-power VLSI design [18].

4. Hybrid Machine Learning Models:

The formal verification of a hybrid machine learning-based fault prediction model in Internet of Things (IoT) applications assures the reliability, safety and robustness of predictive analytics in dynamic environments. Through the integration of classical formal methods with machine learning algorithms, this approach will render both the interpretability of formal verification as well as the adaptability of machine learning models. The use of formal techniques like model checking, theorem proving, and static analysis are employed to ensure the correctness of the predictions which is made by the machine learning model under all possible circumstances and which is also extremely important for safety-critical IoT applications such as healthcare, autonomous systems, and smart grids. The hybrid method not only improves fault prediction correctness but also ensures that the system will perform as expected, even in extreme conditions, with high assurance for safety-critical systems. The same formal verification technique can be quite effectively used to optimize power consumption in VLSI circuits. In VLSI design, power efficiency is a very significant factor, particularly in low-power chips and large-scale integrated circuits. By combining a hybrid machine learning model with formal verification methods, designers are able to accurately forecast the power consumption patterns as well as by ensuring that power management techniques will adhere to design specifications and constraints. For example, machine learning models can forecast power consumption according to workload patterns, whereas formal verification assures that dynamic power scaling techniques (e.g., DVFS) do not breach timing or

operational constraints. This union renders a solid platform for delivering high performance along with low power consumption, thus permitting more efficient and dependable VLSI systems to be designed [19].

Table 1: Comparison of Supervised, Unsupervised, Reinforcement, and Hybrid Machine Learning Models

Feature	Supervised Learning	Unsupervised Learning	Reinforcement Learning	Hybrid Learning
Definition	Models learn from labeled data to make predictions.	Models find patterns in data without explicit labels.	Models learn through trial and error using rewards and punishments.	Combines two or more learning approaches for improved performance.
Data Requirement	It requires labelled data with input-output pairs.	It works with unlabeled data, focusing on finding structures.	It requires an environment with an agent, actions, rewards, and states.	It can utilize labeled, unlabeled, or a mix of data types.
Learning Approach	Learning under supervision using known outcomes.	Learning without supervision to identify hidden patterns.	Learning through interaction with the environment.	Integrates supervised, unsupervised, or reinforcement techniques.
Use Cases	Classification, Regression, Image Recognition, Spam Detection.	Clustering, Anomaly Detection, Market Basket Analysis.	Robotics, Game AI, Autonomous Vehicles, Resource Management.	Semi-supervised learning, Self-supervised learning, Transfer learning.
Advantages	High accuracy with sufficient labeled data, interpretable models.	It can work with raw, unlabelled data, useful for exploratory analysis.	It learns optimal strategies for complex environments.	It leverages strengths of multiple techniques, more flexible.
Challenges	It requires large labeled datasets, potential over fitting.	Less interpretability, difficult to validate results.	It needs well-defined reward mechanisms, may require long training times.	Complexity in model design, computationally intensive.
Example Algorithms	Linear Regression, SVM, Decision Trees, Neural Networks.	K-Means, DBSCAN, PCA, Hierarchical Clustering.	Q-Learning, Deep Q Networks, Policy Gradient Methods.	Semi-supervised SVM, Autoencoders, Transfer Learning Models.

The table 1 represents supervised, unsupervised, reinforcement as well as hybrid machine learning models to highlight their clear learning approaches as well as data requirements. Supervised learning works on labeled data for accurate predictions whereas unsupervised learning uncovers hidden patterns in unlabeled data. Reinforcement learning focuses on learning using interactions with an environment consists of rewards and penalties. Hybrid learning will combine the multiple approaches to increace flexibility as well as performance. Each method here serves specific use cases from classification and it clusters to dynamic decision-making and also adaptive modelling [29] [30].

III. Challenges and Limitations in Power Prediction in VLSI Circuits Using Machine Learning

Power prediction in VLSI circuits based on machine learning is challenged by a number of issues and limitations, which are mainly concerned with data quality, model complexity, and generalization. Availability and accuracy of labeled datasets is one of the major challenges. Power consumption information for VLSI circuits may be hard to get, particularly for new or proprietary designs. Also, simulated datasets may not present realistic conditions to begin with, causing inconsistencies in model applications against real hardware. The high level of transistor complexity in VLSI circuits along with their many interdependencies, also makes extraction and selection a problem. In addition to requiring complex pre-processing techniques owing to the frequently large dimensionality of the input data, the feature selection adds the challenge of opting the appropriate features without leaving the necessary data. Moreover, the employment of complex models is needed due to the non-linear behaviour of power consumption in response to changing operational conditions, which could result in higher training time and also the computing overhead. The drawback here is the capacity of machine learning models to generalize in

power prediction. The Supervised models can generate extremely accurate results on known data but they might not be able to generalize well to unexpected scenarios particularly with new design techniques and to develop VLSI technology. The limitation is the generalization capability of machine learning models in power prediction. While highly accurate results on known data are possible using the models of supervised learning but they may not be able to generalize well to unknown situations especially with emerging VLSI technologies and novel design methodologies. A frequent danger here is overfitting where the model is excellent at predicting from training data but cannot make correct predictions in practical use. Moreover, the interpretability of intricating models like deep learning networks, tends to be low and designers may not easily comprehend how certain design parameters affect power consumption. The integration of machine learning models with current Electronic Design Automation (EDA) tools also poses compatibility as well as implementation issues. These limitations can be addressed through a balanced strategy that involves state-of-the-art data augmentation methods, hybrid model-building approaches and coordination among machine learning researchers and VLSI designers to build robust and power modeling models which will be reliable [20].

A. Data Availability and Quality

The essential factors are the availability and quality of data when creating efficient machine learning models for power prediction in VLSI circuits. The biggest obstacle in this area is collecting large, heterogeneous, and high-quality datasets that well represent the diverse power consumption patterns of various VLSI designs under various operational conditions. Power consumption data from actual operating conditions for proprietary or new VLSI architectures is usually limited by confidentiality issues and intellectual property limitations. Moreover, the creation of synthetic data via simulations can be computationally intensive and may not always preserve the full realism of actual behaviours. Poor data quality in the form of noise, missing values, and biases can also corrupt model performance with consequent inaccurate predictions of power and possible design inefficiencies.

To overcome these issues, data augmentation methodologies can contribute significantly to ameliorate both the quantity and quality of the dataset. Data augmentation refers to the process of generating novel data samples by changing existing data, e.g., scaling, rotation, noise addition or synthesizing novel samples through generative models. For VLSI power prediction, this might involve simulating various workload conditions, environmental variability, or synthetic design parameters. The augmentation not only addresses the issue of small datasets but also increases the strength of the model as it is provided with a greater variety of possible situations. By integrating data augmentation with pre-processing techniques like normalization and feature engineering ensures that the machine learning model is trained using a balanced dataset and finally converting to more accurate and reliable power predictions in VLSI design flows[21].

B. Model Generalization Issues

The Generalization issues in power estimation for VLSI circuits will arise when machine learning models correctly perform on training sets but make incorrect predictions on unseen data or novel circuit designs. Such issues are likely to result from overfitting, whereby the model not only learns the inherent patterns but also the noise as well as anomalies contained in the training set. Overfitted models are characterized by low bias and high variance, i.e., they fit too well to the idiosyncrasies of the training data and are unable to generalize to new situations. This is especially undesirable in VLSI power estimation, where circuit configurations and operating conditions can be very diverse, requiring models that are able to accommodate new inputs without substantial performance loss. The diversity as well as complexity of VLSI circuits further compound model generalization issues. The changes in the process, changing workloads dynamically, and adaptive design architectures represent uncertainty that machine learning models have to manage efficiently. To enhance generalization, methods like cross-validation, regularization, and simplification of complex models can be used. Also, training on diverse as well as representative datasets, along with data augmentation methods, aids in exposing the model to a broad range of situations. Hybrid modeling techniques that integrate machine learning with conventional analytical models can also promote generalization by leveraging domain knowledge during learning. Finally, strong generalization is obtained through a balance between model complexity and robustness rendering consistent power prediction across varying VLSI circuit designs as well as operating environments [22].

C. Computational complexity

Computational complexity is a major factor in using machine learning models for power prediction in VLSI circuits since the models must handle enormous amounts of data produced by complex circuit designs. High-dimensional datasets with hundreds or thousands of features describing design parameters and operating states can easily escalate the computational cost during training and inference. Such complex models, especially deep learning models, need high computational power and time to work through such datasets, which may slow their feasible application in the time-critical VLSI design cycle. Utilizing data mining-based feature selection techniques in power prediction for VLSI circuits can simplify the machine learning models, improving computational efficiency without affecting prediction accuracy. Methods like Principal Component Analysis (PCA), Recursive

Feature Elimination (RFE), and filter-based techniques assist in lowering the dimensionality of the dataset, thereby reducing the time and resources required for model training and inference. These techniques not only enhance processing efficiency but also aid in reducing over fitting risk by concentrating the model on the most significant features. Additionally, integrating discriminative machine learning strategies with efficient feature selection can yield an optimal compromise between model complexity and computational efficiency, resulting in faster and more accurate power estimation in VLSI design flows [23].

D. Integration with EDA tools

Integration with Electronic Design Automation (EDA) tools is an important factor in using machine learning models to predict power in VLSI circuits. EDA tools comprise of a significant role in streamlining many stages of VLSI design, such as synthesis, placement, routing as well as verification. Integration of machine learning methodologies within these processes can go a long way in enhancing predictive accuracy and efficiency especially in power estimation. Nevertheless, smooth integration has a number of challenges that include compatibility with current design flows, computational efficiency as well as generating intelligible results for designers. In order to seamlessly integrate machine learning models into power estimation tools within the EDA environment, the models require to be compatible with the data structures, interfaces and processing models of the EDA ecosystem. This is frequently obtained by embedding machine learning algorithms into the toolchain or by creating plug-ins that can analyze design data in real time. In addition, the integration should be done keeping in mind computational constraints so that the predictive ability introduced does not introduce latency or diminish the overall efficiency of the design process. This method enables a more effective design process allowing engineers to better optimize power consumption and meet design objectives sooner and more efficiently [24].

IV. SUMMARY OF KEY FINDINGS OF PAST STUDIES

The integration with Electronic Design Automation (EDA) tools is an important factor in using machine learning models to predict power in VLSI circuits. EDA tools comprise of a significant role in streamlining many stages of VLSI design, such as synthesis, placement, routing as well as verification. Integration of machine learning methodologies within these processes can go a long way in enhancing predictive accuracy and efficiency especially in power estimation. Nevertheless, smooth integration has a number of challenges that include compatibility with current design flows, computational efficiency as well as generating intelligible results for designers.

In order to integrate machine learning models without difficulties into power estimation tools within the EDA environment, the models require to be compatible with the data structures, interfaces and processing models of the Electronic Design Automation environment. This is often obtained with integration of machine learning algorithms into the tool chain or by creating plug-ins that can analyse design data in real time. In addition, the integration should be done keeping in mind computational constraints so that the predictive ability which is incorporated does not introduce delay or reduce the overall efficiency and performance of the design process. This method enables a more effective and improved design process allowing engineers to better optimize power consumption and meet design objectives to fulfil design objectives sooner and more efficiently [25].

The machine learning methods for predictive modeling of power usage in VLSI design has become more and more important in achieving power efficiency and also for design optimization. The Predictive Modelling for Power Consumption in VLSI Design using methodologies like Linear Regression, Random Forests and Neural Networks can efficiently ameliorate the accuracy of prediction of power consumption in VLSI circuits. Linear Regression renders an easy method to model the interaction between design parameters and power consumption, giving immediate feedback in early stages of the design process. Random Forests, through ensemble learning, enhance the stability of predictions and address high-dimensional data by combining multiple decision trees' outputs. Neural Networks, and specifically deep architectures, are superior at modeling non-linear and subtle dependencies in high-dimensional and large design datasets. By incorporating such machine learning models into computer-aided design (CAD) platforms, designers will be able to obtain predictive insights early in the design cycle that will allow them to make power-efficient decisions. This does not only minimize the risk of expensive design iterations but also enables the design of more efficient and reliable semiconductor devices [26].

Decreasing computational complexity without compromising performance is a key objective in using deep learning methods for VLSI power prediction and optimization. The reinforcement learning with deep neural networks provides a promising solution to this balance. The method is presented to decrease model complexity by reducing the number of channels in deep neural networks proving that this approach maintains predictive accuracy while drastically reducing computational demands. This methodology is specifically applicable in VLSI design where computational effectiveness is essential to incorporate machine learning models into Electronic Design Automation (EDA) tools efficiently. Through the optimization of deep learning models' architecture by reinforcement learning methods, designers are capable to design lightweight yet effective models that render precise power consumption estimates without creating too much computational overhead. This efficiency-performance load balance facilitates accelerated design

iteration as well as promotes the usability of machine learning-based power optimization in the design flows of contemporary semiconductors [27].

The application of Artificial Intelligence (AI) and Machine Learning (ML) in VLSI design is crucial in the creation of VLSI systems more energy efficient and supporting sustainable development specifically for smart cities. It uses advanced machine algorithms like Regression Models, Gradient Boosting, and XGBoost that can really minimize power usage in VLSI circuits. These algorithms render strong predictive power for energy usage estimation which supports enhanced decision-making in the design stage. Gradient Boosting and XGBoost stand out for their ability to manage complicated high-dimensional data through iterative refinement using boosting methods. This integration of AI and ML not only optimizes the power efficiency of VLSI design processes but also it is connected to the general objective of optimizing smart grid performance and advancing sustainable urban infrastructure. The ability to predict as well as manage power usage effectively facilitates more intelligent resource planning and aids to build eco-friendly and more energy-efficient cities [28].

It has been explained in the table given below:

Table 2 Summary of Key findings of past studies

Machine Learning Method	Strengths	Challenges	Integration in EDA Tools	Impact on Power Optimization
Linear Regression	Simple, interpretable, provides quick feedback in early design stages	Limited to linear relationships, may not capture complex dependencies	Easily integrated for early-stage power estimation	Facilitates quick power estimation and early design decisions
Random Forests	Stable predictions, handles high-dimensional data efficiently	Can be computationally expensive with large datasets	Useful for feature selection and robust predictions	Improves stability and accuracy in complex designs
Neural Networks	Models complex nonlinear relationships, suitable for large datasets	High computational cost, requires large datasets for training	Best for high-accuracy power modeling with deep learning support	Allows for high-fidelity power predictions
Reinforcement Learning with Deep Neural Networks	Balances computational efficiency and predictive accuracy	Needs careful tuning to optimize efficiency without losing accuracy	Optimizes neural networks to reduce computational overhead	Balances computational complexity with prediction accuracy
Gradient Boosting	Handles high-dimensional data, robust predictive capability	Prone to overfitting if not carefully tuned	Enhances energy efficiency predictions in smart grids	Supports energy-efficient designs with iterative refinement
XGBoost	Efficient boosting method, strong predictive power	Requires extensive hyperparameter tuning for best performance	Ideal for refining power estimation with boosting techniques	Optimizes power efficiency for VLSI circuits and smart city applications

V. Conclusion

Machine learning will offer a promising approach for power estimation in CMOS VLSI circuits by rendering fast, accurate, and efficient predictions during the design phase. By leveraging data-driven models, this approach performs better than traditional simulation methods in both speed and precision and thus it enables designers to optimize circuit performance as well as to reduce power consumption effectively. The integration of machine learning in VLSI design not only improves the development process but it also opens new possibilities for the enhancement of efficiency and sustainability of modern electronic devices. Future research here focus on refining these models as well as exploring new machine learning techniques to further ameliorate the accuracy of power estimation and adaptability. Ultimately, it sets a strong foundation for the advancement of smart, power-efficient electronic designs in a fast technology-driven world. It will also facilitate the innovation in advanced technologies like IoT, AI and portable devices by optimization of power management in increasingly complex circuits.

REFERENCES

[1] Davari, B., Dennard, R. H., & Shahidi, G. G. *CMOS scaling for high performance and low power-the next ten years.* Proceedings of the IEEE, 1995, 83(4), 595-606.

[2] Amuru, D., Zahra, A., Vudumula, H. V., Cherupally, P. K., Gurram, S. R., Ahmad, A., & Abbas, Z. *AI/ML algorithms and applications in VLSI design and technology*. Integration, 2023, 93, 102048.

[3] Ande, J. R. P. K. R., & Khair, M. A. *High-Performance VLSI Architectures for Artificial Intelligence and Machine Learning Applications.* International Journal of Reciprocal Symmetry and Theoretical Physics, 2019, 6(1), 20-30.

[4] Saurabh, S., Jain, P., Agarwal, M., & Ram, O. S. *Applications of Machine Learning in VLSI Design.* In VLSI and Hardware Implementations Using Modern Machine Learning Methods 2021, pp. 125-139, CRC Press.

[5] Choubey, A., & Choubey, S. B. *Machine Learning for Testing of VLSI Circuit.* In VLSI and Hardware Implementations Using Modern Machine Learning Methods 2021, pp. 23-40, CRC Press.

[6] Amuru, D., Zahra, A., Vudumula, H. V., Cherupally, P. K., Gurram, S. R., Ahmad, A., & Abbas, Z. *AI/ML algorithms and applications in VLSI design and technology*. Integration, 2023, 93, 102048.

[7] Zhang, Y., & Demosthenous, A. *Integrated circuits for medical ultrasound applications: Imaging and beyond.* IEEE Transactions on Biomedical Circuits and Systems, 2021, 15(5), 838-858.

[8] Shreyanth, S., Harshitha, D. S., & Niveditha, S. *Implementation of machine learning in VLSI integrated circuit design.* SN Computer Science, 2023, 4(2), 137.

[9] Lauwers, E., & Gielen, G. *Power estimation methods for analog circuits for architectural exploration of integrated systems.* IEEE transactions on very large scale integration (VLSI) systems, 2002, 10(2), 155-162.

[10] Nurul Adlina, J. *Complementary metal-oxide-semiconductor (CMOS) charge pump with temperature variation for self-powered applications (Doctoral dissertation, UTAR)*, 2023.

[11] Nasser, Y., Lorandel, J., Prévotet, J. C., & Hélard, M. *RTL to transistor level power modeling and estimation techniques for FPGA and ASIC: A survey.* IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 40(3), 479-493.

[12] Nemani, M., & Najm, F. N. *High-level area and power estimation for VLSI circuits.* IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1999, 18(6), 697-713.

[13] Poovannan, E., & Karthik, S. *Pre Synthesis and Post Synthesis Power Estimation of VLSI Circuits Using Machine Learning Approach*. Applied Artificial Intelligence, 2022, 36(1), 2145640.

[14] Jung, H., & Pedram, M. *Supervised learning based power management for multicore processors.* IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29(9), 1395-1408.

[15] Verma, R., Nagar, V., & Mahapatra, S. *Introduction to supervised learning.* Data Analytics in Bioinformatics: A Machine Learning Perspective, 2021, 1-34.

[16] Aboah Boateng, E., & Bruce, J. W. *Unsupervised machine learning techniques for detecting PLC process control anomalies*. Journal of Cybersecurity and Privacy, 2022, 2(2), 220-244.

[17] Varghese, M. P., & Muthumanickam, T. Machine Learning Techniques to Evaluate the Approximation of Utilization Power in Circuits.

[18] Li, X., Chen, L., Chen, S., Jiang, F., Li, C., Zhang, W., & Xu, J. *Deep Reinforcement Learning-Based Power Management for Chiplet-Based Multicore Systems.* IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2024.

[19] Souri, A., Mohammed, A. S., Potrus, M. Y., Malik, M. H., Safara, F., & Hosseinzadeh, M. *Formal verification of a hybrid machine learning-based fault prediction model in Internet of Things applications.* IEEE Access, 2020, 8, 23863-23874.

[20] Barbierato, E., & Gatti, A. *The challenges of machine learning: A critical review.* Electronics, 2024, 13(2), 416.

[21] Srivastava, P., Kumar, P., & Abbas, Z. *Qualitative data augmentation for performance prediction in VLSI circuits*. Integration, 2024, 97, 102186.

[22] Hutchins, J., Alam, S., Zeumault, A., Beckmann, K., Cady, N., Rose, G. S., & Aziz, A. *A generalized workflow for creating machine learning-powered compact models for multi-state devices.* IEEE Access, 2022, 10, 115513-115519.

[23] Bajaj, K., & Arora, A. *Improving the intrusion detection using discriminative machine learning approach and improve the time complexity by data mining feature selection methods.* International Journal of Computer Applications, 2013, 76(1).

[24] Goswami, P., & Bhatia, D. *Application of machine learning in FPGA EDA tool development.* IEEE Access, 2023, 11, 109564-109580.

[25] Elfadel, I. M., Boning, D. S., & Li, X. (Eds.). *Machine learning in VLSI computer-aided design*, 2019, pp. 0278-0070, Cham: Springer.

[26] Arya, A. *PREDICTIVE MODELLING FOR POWER CONSUMPTION IN VLSI DESIGN USING MACHINE LEARNING*. ACTA SCIENTIAE, 2024, 7(1), 659-669.

[27] Agha, S., Nazir, S., Kaleem, M., Najeeb, F., & Talat, R. *Performance evaluation of reduced complexity deep neural networks.* PLoS ONE, 2025.

[28] Singh, B., & Raghav, A. *Artificial Intelligence and Machine Learning in VLSI: Projecting Energy Management towards Sustainability in Smart Cities.* In Role of Internet of Everything (IOE), VLSI, 2025.

[29] Homod, R. Z., Togun, H., Hussein, A. K., Al-Mousawi, F. N., Yaseen, Z. M., Al-Kouz, W., ... & Hussein, O. A. *Dynamics analysis of a novel hybrid deep clustering for unsupervised learning by reinforcement of multi-agent to energy saving in intelligent buildings.* Applied Energy, 2022, 313, 118863.

[30] Homod, R. Z., Togun, H., Hussein, A. K., Al-Mousawi, F. N., Yaseen, Z. M., Al-Kouz, W., ... & Hussein, O. A. *Dynamics analysis of a novel hybrid deep clustering for unsupervised learning by reinforcement of multi-agent to energy saving in intelligent buildings.* Applied Energy, 2022, 313, 118863.